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# power

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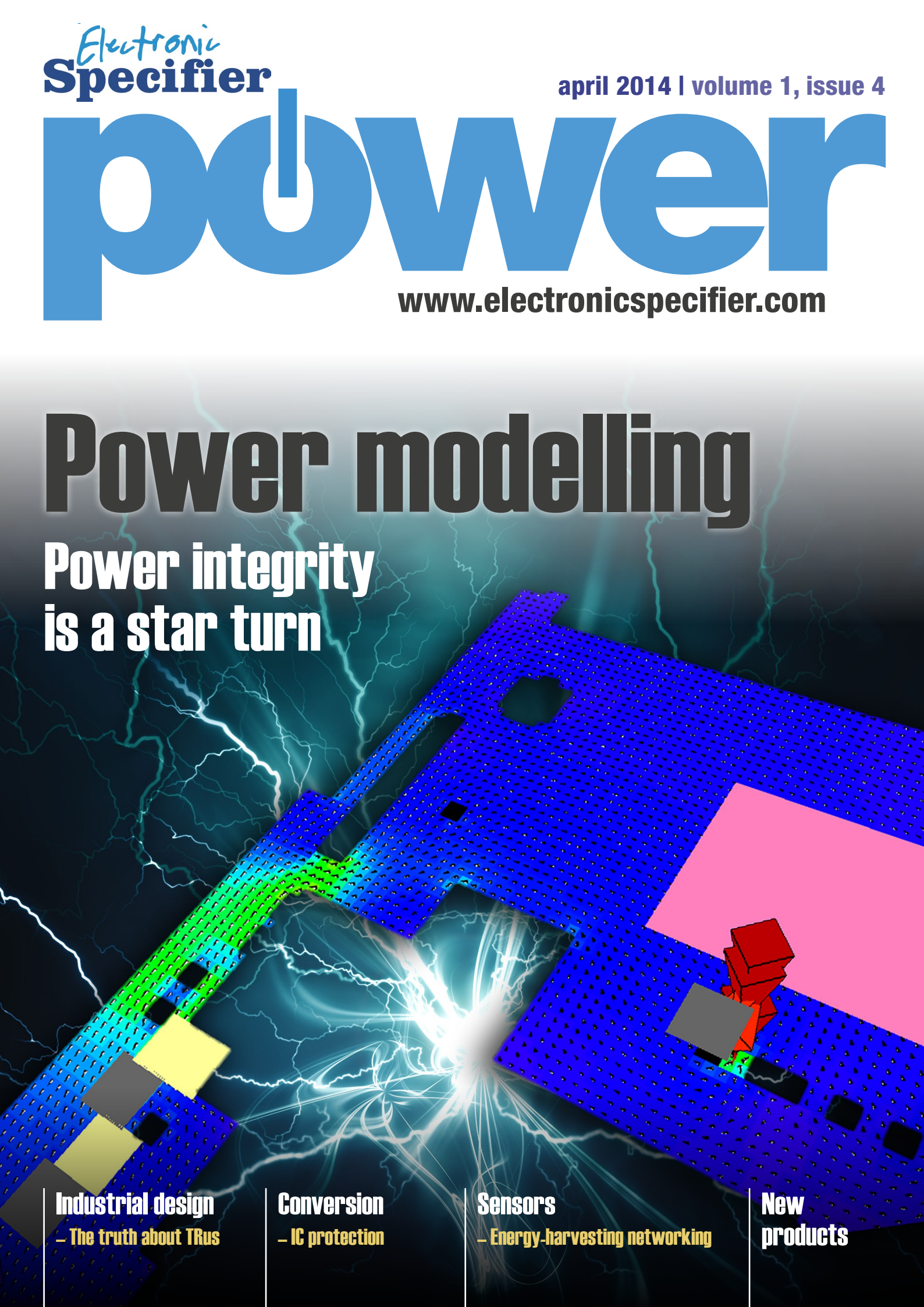
# Power modelling

## Power integrity is a star turn



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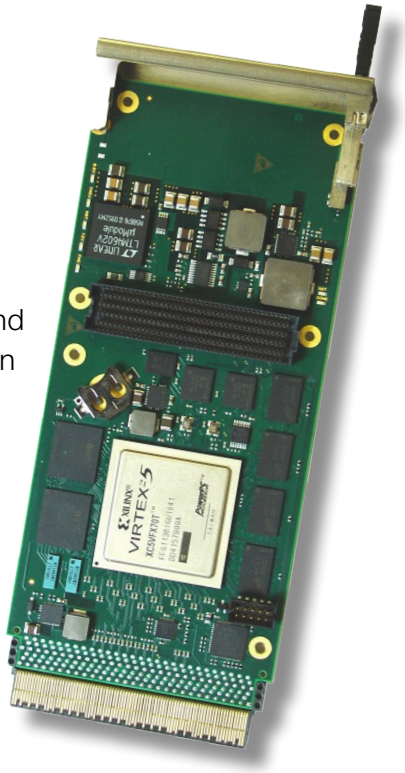
# Power integrity module is a star turn

**TEWS reduced development time and cost of complex high-speed PCBs using concurrent power integrity simulation. Michael Költzow, TEWS Technologies explains how it was done.**

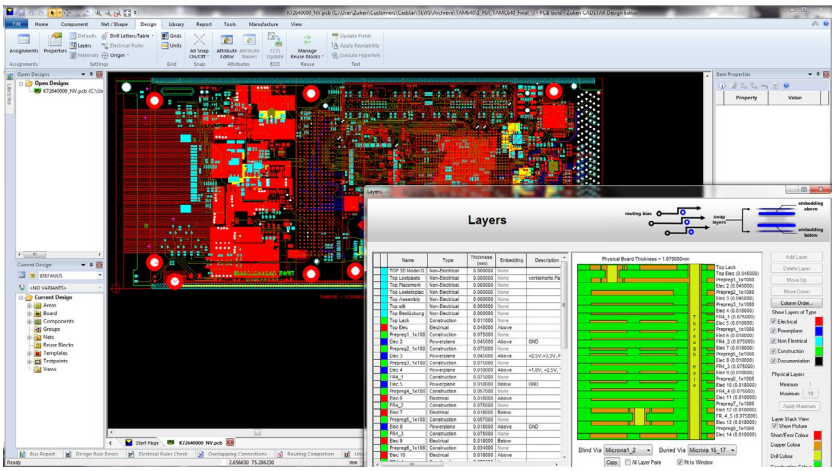
Like many companies working with FPGA-based boards, TEWS Technologies, the embedded interface manufacturer based in Hamburg, faces increasing power integrity challenges due to the multiple voltage rails needed by ICs. Today's designs can contain dozens of power distribution networks (PDNs), creating complex design scenarios for the engineers who have to make them work. In addition, they needed to meet the highly complex impedance targets and decoupling requirements specified by semiconductor vendors, while still complying with signal integrity rules.

The company has been using Zuken's CADSTAR for its PCB design process, increasing their use of different high-speed options in recent years, using tools such as advanced high-speed modules for constraint management and constraint-driven routing, and signal integrity simulation in pre- and post-layout phases.



TEWS interface card.

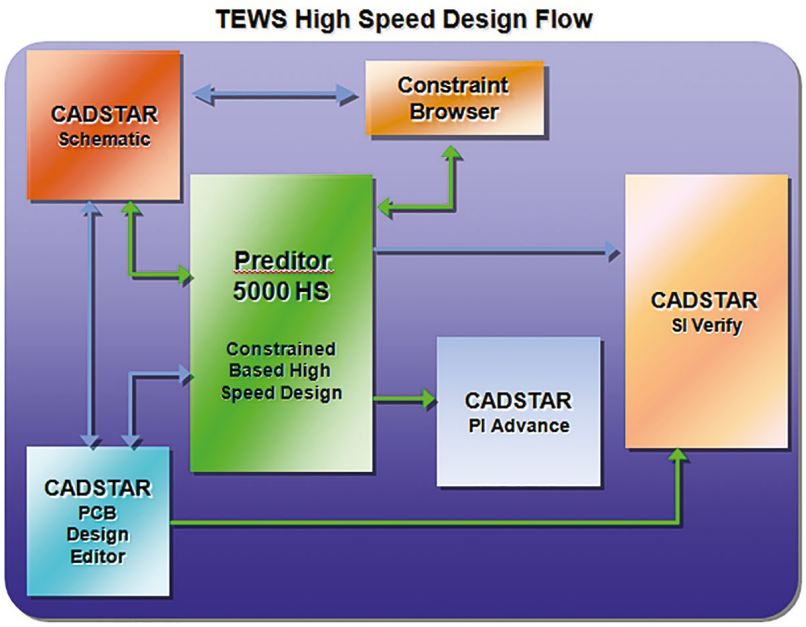
The company recently added CADSTAR Power-Integrity Advance module to the high-speed design flow to address design problems around power distribution on PCBs.




## Acting early in the design phase

Ralf Brüning, senior product specialist for high-speed and analysis tools at Zuken EMC Technology Center Paderborn, Germany, worked alongside TEWS in the initial implementation to ensure smooth setup of the new analysis module. Several initial projects were designed to shorten the tool introduction phase, and Ralf made sure there was close cooperation in the initial stages.

"We had been working with TEWS for a number of years, which made getting the project up and running much easier. Having an established high-speed process




High speed design flow

in place also made it more straightforward when it came to enhancing the design process analysis capability, as for example information such as IBIS models were already available for each new design."

To verify signal integrity, TEWS compared the simulation and impedance results with measurements performed by their board manufacturers. Then they compared the Power Integrity Advance analysis results with analytical attempts on specially designed structures. The company was pleased by the match between the simulation results and measurements and gained confidence in the power integrity simulation capabilities as well.

It is essential that correct signal routing and bus termination is guaranteed to ensure reliable operation. The impedance-controlled layer and target of 55Ω needed to closely match PCB specifications for SI and power distribution systems.

## Tight integration

The Zuken SI Verify and Power Integrity Advance tools were quick and easy to use from the outset. TEWS soon began to take advantage of a recently added link from Constraint Manager and high-speed routing into the Power Integrity Advance tool that allows the design engineer to perform power integrity analysis (AC and decoupling analysis, as well DC investigations) prior to full board routing. This supports a virtual power integrity prototyping environment in which the designer can test different design options without the delay and cost of creating a full prototype.

Integrating signal integrity or power integrity tools into a CAD design environment often involves a translator that extracts the design database and creates intermediate files for the analysis. The resulting design process can be cumbersome: the engineer must export a design file, invoke the analysis software, make notes of the results, return to the design tool to make adjustments, and then repeat this process until an acceptable solution is found.

## Integration

The integrated Signal Integrity and Power Integrity analysis modules offer a more streamlined alternative. The engineer invokes the simulator from the PCB CAD tool, works on selected elements, or even the entire design, makes design changes and immediately re-analyses the results.

"This is a much higher level of integration than has previously been possible with third-party analysis solutions. It lets us integrate analysis very early in the design process; a capability that is becoming increasingly critical to a project's success," said Peter Zimmermann, head of hardware design, TEWS.

With power integrity analysis linked directly to the CADSTAR constraint-based PCB design process, the design can be re-simulated during or after each layout step to ensure no problems have been introduced.

## EMI compliance

TEWS soon realised that they were able to try different decoupling schemes, layer spacing and power distribution area layout schemes using “what-if” capabilities. The company supplies products to international markets, so EMI and EMC compliance are also critical. This requirement was satisfied by using the EMI module within the Power Integrity Advance toolset, using algorithms developed at Missouri University of Science and Technology (formerly the University of Missouri-Rolla), to predict the worst-case emission levels of a PCB.

***CAD designers are able to perform power integrity analysis during the power distribution layout ensuring sufficient power is being delivered to all ICs.***

Even though the company did not expect to match chamber measurement with accurate dBs, the ease-of-use and reliability of the results of Power-Integrity Advance EMI, together with its fast analysis, gave important hints about radiation hot spots on the board well before the first prototype.

## Decoupling reduction

Since integrating Power Integrity Advance in design flow, TEWS has realised its goal of designing a PDN capable of providing charge to all the ICs on a minimal number of PCB layers. CAD designers are able to perform power integrity analysis during the power distribution layout and work closely with electronics engineers to ensure that sufficient power is being delivered to all ICs. Design changes may then dictate changes to PDNs and/or the placement of capacitors on the PCB.

Designers were confident the layer stack-up that matched the PDN impedance target, an optimal power-net routing and an effective decoupling scheme – even before manufacturing the first board. Prototypes testing agreed with what had been experienced using Zuken’s simulation tools.

Creating more right-the-first-time designs, the company reports that another benefit is being able to reduce the number of decoupling capacitors, which adds up to a significant reduction in manufacturing costs.

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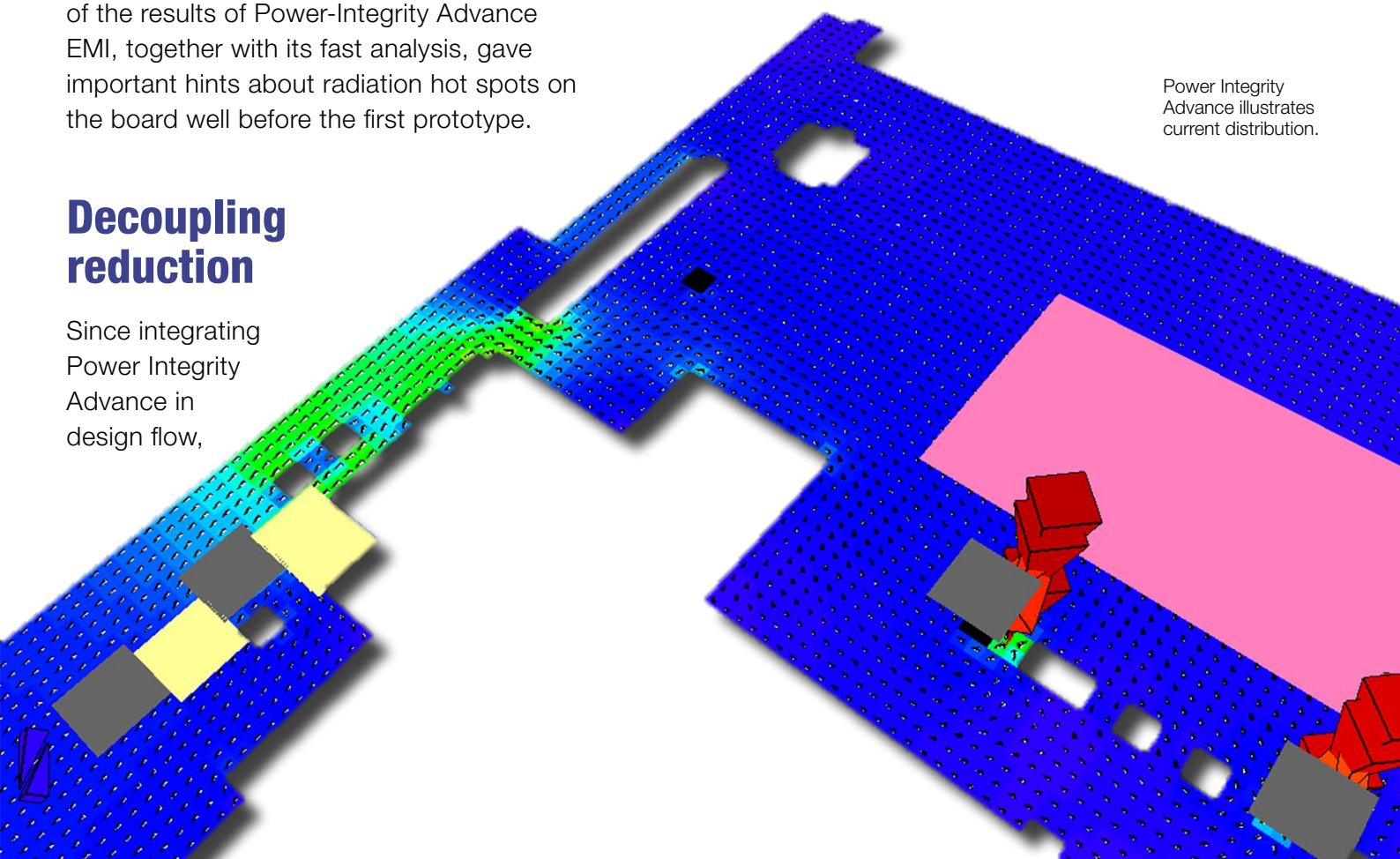

Power Integrity Advance illustrates current distribution.